Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**DRAFT**

**PAD FUNCTION:**

1. **GND**
2. **INPUT +**
3. **INPUT –**
4. **VEE**
5. **BAL**
6. **BAL/STROBE**
7. **OUTPUT**
8. **VCC**

**.061”**

**5**

**4**

**3**

**8 1 2**

**7 6**

**.049”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size = .004” X .004”**

**Backside Potential: FLOATING**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .049” X .061” DATE: 11/9/21**

**MFG: TEXAS INSTRUMENTS THICKNESS .00?” P/N: LM111**

**DG 10.1.2**

#### Rev B, 7/1